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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,282	03/30/2004	Yasutaka Nakashiba	8008-1052	2273

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EXAMINER	
JACKSON JR, JEROME	

ART UNIT	PAPER NUMBER
2815	

MAIL DATE	DELIVERY MODE
01/30/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,282	NAKASHIBA, YASUTAKA	
	Examiner	Art Unit	
	Jerome Jackson Jr.	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-8,13,16 and 23-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8,13,16 and 23-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-4,6-8,13,16,23-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudo in view of O and further in view of applicant's prior art admissions.

The new limitations in claim 1 reciting three diffusions in MOS wells and the "varactor element" having the thinnest gate insulating film do not structurally distinguish over the applied art. See column 11 of O where varactors using N-Well MOSFET design are disclosed, and further, varactor design with thinner gate logic MOSFET devices (in contrast with thicker gate I/O MOSFET devices) are disclosed:

"Varactors are used for tuning filters and implementing low phase noise voltage controlled oscillators (VCO). A varactor is a semiconductor device (often a FET) in which the capacitance is sensitive to the applied voltage. A varactor can be formed by positioning an NMOS transistor in an n-well [C.-M. Hung, I-C. Wu, Y.-C. Ho, and K. K. O, "High Q Capacitors (>150 @900 MHz) Implemented in a CMOS Process for Wireless Applications," IEEE Transaction on MTT, vol. 46, no. 5, pp 505 511, May, 1998.]. This arrangement creates a short between the source, well and drain.

(59) At 24 GHz, the varactor Q is expected to be about 30, which will limit the performance of filters and the VCO. When the frequency is increased beyond 24 GHz, the situation will become worse.

(60) CMOS varactors are generally formed using design rules applicable for logic devices, as opposed to design rules for input/output (I/O) devices. Logic devices are generally significantly smaller than I/O devices, and use a thinner gate oxide."

Hence, O discloses the claimed structure where thinnest gate dielectric "varactors" are integrated with thicker gate dielectric I/O MOSFETs. Note all the elements of a radio are integrated on the same chip in O, therefore thin gate dielectric varactors integrated on the same chip with thick gate I/O MOSFETs are obvious from O.

Kudo further shows how different thickness gate dielectrics can be made in CMOS technology, and applicant's prior art admissions further discloses how varactors can be made and designed from CMOS devices. Together the references disclose the claimed subject matter and there are no unexpected results.

Claims reciting particular thicknesses for the gate dielectrics are not patentable because the prior art teaches the general conditions of adjusting or choosing the thicknesses of the gate dielectrics to achieve the desired capacitance, and uses submicron device dimensions, and there are no unexpected results from applicant's particular choice of thickness which is considered routine for submicron dimensions, as we have here, absent unexpected results.

Claims reciting voltage potentials or functional language (forms a varactor) likewise are not patentable as the prior art applies voltage potentials and functions in the same manner.

Applicant's arguments filed 11/08/07 have been fully considered but they are not persuasive. Applicant argues the prior art does not disclose thinner gate dielectrics for varactors. This argument is not convincing, as shown above, O discloses thinner gate dielectrics (logic MOSFETs) for varactors, and thicker gate dielectrics for I/O MOSFETs.

Arguments regarding three diffusions and well structure are not convincing of patentability as applicant's own admissions disclose routine varactor design using CMOS wells and three diffusions. Likewise O discloses routine varactor design with wells and diffusions as shown above.

Arguments regarding the varactor design as not corresponding to a MOS transistor are unconvincing of patentability as the prior art applied disclose the claimed varactor structure.

Arguments regarding O not teaching "the claimed relationship between the CMOS gate oxide film thickness and the VCO gate oxide film thickness" are unconvincing as shown above in the quotation from O where thin gate dielectric (logic gate size MOSFET) varactors are integrated with thick gate dielectric I/O MOSFETs.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jerome Jackson Jr. whose telephone number is 571-272-1730. The examiner can normally be reached on M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jj

JEROME JACKSON
PRIMARY EXAMINER